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(54) Title: LITHOGRAPHY SYSTEMS EMPLOYING PROGRAMMABLE RETICLES

(57) Abstract

A programmable reticle is disclosed for use in transferring patterns to wafers in a photolithography system. The programmable reticle is provided as a medium having a two-dimensional array of electronically controllable elements, each of which can be made either transparent or opaque as dictated by an electronic signal. Collectively, the opaque elements of the reticle define a mask layout pattern. The programmable reticle forms part of a complete photolithography system including a radiation source which shines onto the reticle, a stepper which directs radiation from the reticle onto a wafer, and a programmable control system for defining the mask provided on the programmable reticle. For most applications, the elements of the two-dimensional array are no larger than about ten microns.

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LITHOGRAPHY SYSTEMS EMPLOYING PROGRAMMABLE RETICLES

Background of the Invention

The present invention relates to photolithography systems for forming integrated circuits. More specifically, the invention relates to programmable reticles and systems employing such reticles for streamlining integrated circuit development and fabrication.

Photolithography is a widely used process in the integrated circuit fabrication industry. In fact, whenever a pattern must be transferred to a semiconductor wafer, a photolithography process is employed. Photolithography systems have evolved into highly complex systems for optically projecting such patterns onto wafers with micron to submicron resolution. Current integrated circuit fabrication processes may employ fifteen or more separate photolithography steps in the fabrication of a single integrated circuit.

Whenever a new pattern must be transferred to a wafer, ultraviolet light or some other form of radiation is shown through a reticle and projected onto a photosensitive layer on a wafer surface. A reticle is a plate having transparent and opaque regions which are arranged to define a mask pattern layout. The regions of the photosensitive layer that are exposed to light are selectively retained or removed (depending upon the chemical nature of the photosensitive layer) in a subsequent development step. The mask pattern is ultimately transferred to the underlying substrate and the exposed regions are transformed by a process such as ion implantation or etching. Unfortunately, each new pattern transferred to the wafer requires a new reticle.

Figure 1 illustrates a typical process flow 2 for developing an integrated circuit. As shown there, the development process begins at 4, and thereafter at a step 6, an integrated circuit is designed. It should be understood that such integrated circuit is designed solely by software means. Initially, the design exists only in a Boolean representation, and thereafter, it is converted to a multi-level circuit layout to be provided on a wafer. Associated with this layout is a series of mask designs that represent actual patterns to be imposed on the wafer. The mask designs, which are the output of process step 6, are generated in a process known as "tape-out."

The mask designs are electronically transferred to a reticle or photomasking company which performs a manufacturing electron beam exposure system ("MEBS"), step 8, to generate a reticle corresponding to the design. In essence, this step takes the electronic version of the mask and converts it to a physical version. This is a rather complex and expensive process in which an electron beam is moved over an electrostatic medium as specified by the electronic representation of the mask. The output of this process is a reticle having transparent and translucent regions corresponding to the mask layout. In visible and ultraviolet photolithography, the translucent regions may be defined by chromium or chromium oxide on a glass substrate, for example. In

other, more advanced, photolithography processes such as X-ray lithography, a beryllium media may be used.

At the conclusion of the MEBS step 8, a reticle is available and is provided for use in a photolithography step 10. As explained above, this photolithography step involves illuminating the wafer through the reticle to transfer the mask pattern onto the wafer, and thereby generate exposed regions for subsequent processing. At the conclusion of wafer fabrication step 10, a wafer testing step 12 is performed. And at the conclusion of this step, it will be known whether the wafer is suitable for its intended purpose. The associated decision is represented by decision step 14 in process 2. If the wafer is found suitable, the process is simply concluded at 16. In other words, the mask design is adequate for the task at hand. If, on the other hand, it is determined that the wafer has a problem related to the mask design, the process must return to step 6 where the mask is redesigned. Thereafter, the reticle must be formed at step 8, and wafer fabrication and testing must be performed at steps 10 and 12 as described above. Unfortunately, this scenario is rather common in modern chip design. It is very tedious, time consuming, and expensive to regenerate the reticles for each new cycle of this process. In particular, MEBS step 8 is particularly resource intensive.

Thus, it would be desirable to provide a process in which the integrated circuit development process could be made more efficient.

Summary of the Invention

The present invention fills the above need by providing programmable reticles for use in photolithography systems. A programmable reticle is provided as a medium having a two-dimensional array of electronically controllable elements, each of which can be made either transparent or opaque as dictated by an electronic signal. Collectively, the opaque elements of the reticle define a mask layout pattern. In preferred embodiments, the programmable reticle forms part of a complete photolithography system including a radiation source which shines onto the reticle, a stepper which directs radiation from the reticle onto a wafer, and a programmable control system for defining the mask provided on the programmable reticle. For most applications, the elements of the two-dimensional array will be no larger than about ten microns.

By providing a programmable reticle, the invention greatly simplifies the photolithography process. No longer is it necessary to prepare a new reticle by MEBS whenever a new pattern is to be provided to a wafer. Once the programmable reticle is positioned with respect to the source of radiation and the stepper, each new mask is provided by simply reprogramming the reticle elements. In addition, the programmable reticle need not be realigned after each new mask is generated, thus reducing the time required to prepare a photolithography system for exposure. Thus, error correction in photolithography can be conducted "on the fly" during a manufacturing or design. The integrated circuit manufacturer no longer has to have a

new reticle prepared each time that an error is detected. In addition, the mask layouts for a new integrated circuit design can be transmitted directly from the designer's computer system to a photolithography system in accordance with this invention.

In one aspect, the present invention provides a photolithography system for fabricating integrated circuits on a semiconductor substrate. The system can be characterized as including the following elements: (1) one or more stations for providing mask layout data defining features of an integrated circuit on the semiconductor substrate; (2) a programmable reticle in communication with one or more of the stations such that it receives mask layout data; (3) a radiation source aligned to provide radiation through the programmable reticle; and (4) an optical system for directing radiation passing through the programmable reticle onto a radiation-sensitive masking material on the semiconductor substrate such that regions of the radiation-sensitive masking material corresponding to the mask layout data are exposed to said radiation. As explained, the programmable reticle will have an array of elements, each of which can be switched to either a transparent or an opaque state in response to the mask layout data. The radiation from the radiation source will be blocked by those elements in the opaque state and transmitted by those elements in the transparent state.

In preferred embodiments, the lithography system will have multiple stations each configured to provide mask layout data. Some of these stations may even be provided at locations remote from the programmable reticle, possibly at other cites within an enterprise. In such systems, a server may be required to communicate with the one or more stations to control the timing of the information provided to the programmable reticle. Typically, the stations will be workstations or computer terminals adapted to communicate mask layout data to the server.

Another aspect of the present invention provides a method for using photolithography to fabricate integrated circuits on a semiconductor substrate. In this aspect, the method can be characterized as including the following steps: (1) programming a programmable reticle (of the type described above) to define a mask layout; (2) directing radiation onto the programmable reticle such that the radiation passes through the elements of that reticle that are in a transparent state, and the radiation is blocked by the elements that are in an opaque state; and (3) directing the radiation pattern that the passes through the programmable reticle onto a radiation sensitive layer (typically a photoresist) on the semiconductor substrate, so as to expose the pattern of the mask layout onto the radiation sensitive layer. Thereafter, the radiation sensitive layer will be processed in the usual manner to produce a mask on the wafer. After the mask has been formed, the exposed regions of the wafer will be transformed by one of many possible integrated circuit fabrication processes such as ion implantation, etching, etc. In preferred embodiments, the above steps will be repeated numerous times in order to form the integrated circuit.

It is an envisioned that some steps of the overall process may employ traditional non-programmable reticles. In such embodiments, other steps would, of course, employ the programmable reticles of this invention.

These and other features and advantages of the present invention will be described in more detail below with reference to the associated figures.

Brief Description of the Drawings

Figure 1 is a flow chart illustrating a process for generating and using conventional reticles.

Figure 2 schematically illustrates the layout of a preferred embodiment of the present invention in which a programmable reticle is employed in a system having a stepper, a wafer, a server, and various stations connected to the server.

Figure 3 shows a programmable reticle of this invention as it might appear when programmed to provide multiple mask layouts for different dies on a given wafer.

Detailed Description of the Preferred Embodiments

Referring now to Figure 20, a programmable photolithography system 2 is shown. The system 20 includes a radiation source 22 which may be a visible, ultra-violet, x-ray, an electron beam or other source as is known in the art. For visible or ultra-violet radiation, the source may be, for example, a filtered mercury arc lamp or an appropriate laser. Radiation from radiation source 22 is directed through a programmable reticle 24 having an array of controllable elements or pixels, each of which can be switched between a transparent state and an opaque state in response to electronic signals. In general, the controllable elements of the reticle may be made from any media which can be electrically programmed to change their transmittance to the radiation. If visible or ultra-violet radiation is provided by source 22, then programmable reticle 24 is preferably a liquid crystal diode array. However, other programmable media may be employed as well. For example, electrochromic materials which alternate between transparent and translucent states by reversible electrochemical reactions may also be used. Other media may be appropriate x-ray sources.

Radiation passing through programmable reticle 24 is directed onto a wafer 28 by stepper 26. Wafer 28 is held on a support 30 which may move the wafer by translation, rotation, or tilt. In this manner, various regions of wafer 28 are illuminated at different times. The stepper 26 contains the optical and mechanical elements necessary to take the mask image provided by source 22 through reticle 24, maintain or reduce the image as necessary, and provide the image to a photosensitive layer on wafer 28. In preferred embodiments, the stepper 26 will reduce the image

from reticle 24 by 1x, 5x, or 10x. Thus, the resolution required of programmable reticle 24 preferably should be between about 1x and 10x greater than the line width required of integrated circuits fabricated on wafer 28. Thus, for many applications, the largest dimension of the elements (e.g., a diagonal) of the reticle should be at most about 10 micrometers.

In general, the programmable reticles of this invention may be employed in any photolithography system, including projection scanners, projection step-and-repeat machines (steppers), and contact/proximity aligners. In a projection scanner, the entire wafer is exposed in a succession of scans throught the reticle. In a contact/proximity aligner, the programmable reticle is located directly above (to within a few millimeters) or in contact with the wafer. Exposure systems for photolithography are known in the art and are discussed in, for example, chapter 8 of "Integrated Circuit Fabrication Technology", second edition, by D. Elliott, McGraw-Hill Publishing Company, New York, New York (1989). This book is incorporated herein by reference, in its entirety, for all purposes.

Typically, the wafer will be coated with a radiation sensitive photoresist. If a "positive" photoresist is employed, the layer of photoresist becomes bond-broken where the radiation strikes it, thereby rendering it largely soluble in appropriate solvents. The mask is then immersed in or otherwise exposed to a solvent which dissolves those portions of the photoresist layer which are not cross-linked and leaves intact those portions of the photoresist layer which are cross-linked. Thereafter, the mask is exposed to an etchant for an underlying masking layer which either does not attack the remaining photoresist or attacks it very slowly whereby the masking layer may be removed every place where it is not protected by the retained portions of the photoresist. A "negative" photoresist, in contrast, becomes insoluble in appropriate solvent only in those regions where it is exposed to radiation. Of course, both positive and negative photoresists can be employed with the present invention.

After the mask is defined on the wafer, it is further processed such that exposed regions are transformed by ion implantation, etching, or other step employed in integrated circuit manufacture. Generally integrated circuit fabrication employs multiple photolithography steps. Thus, the fabrication process will typically involve repeating the steps of (a) programming the programmable reticle, (b) directing radiation onto the programmable reticle, (c) directing the radiation pattern onto the radiation sensitive layer, (d) removing regions of the radiation sensitive layer, and (e) transforming unmasked regions of the wafer to thereby form an integrated circuit.

In some embodiments, conventional, non-programmable reticles may be used in conjunction with the programmable reticles of this invention. In such cases, it may prove more convenient to use the non-programmable reticles for specified masking steps. For example, in one embodiment, a programmable reticle is reserved for forming interconnect masks, while non-programmable reticles are employed to form all other types masks. This situation may be

appropriate when the programmable reticle is provided on a medium having resolution insufficient to mask the finer features of an integrated circuit.

As noted above, one problem with conventional photolithography technology is that reticles must be replaced whenever a new mask is required in fabricating an integrated circuit. This requires that a new reticle be very carefully aligned between radiation source 22 and stepper 26. Otherwise, features at different levels of the integrated circuit will not be properly aligned, thereby rendering the integrated circuit useless. One important advantage of the present invention is that this reticle aligned procedure is no longer necessary between each photolithography step. This is because programmable reticle 24 is always maintained in fixed alignment between radiation source 22 and stepper 26, regardless of the mask layout required by the process at hand.

The input to programmable reticle 24 is provided by one or more of a series of data generation stations such as stations 32, 34, and 36 shown in Figure 2. These stations, either alone or collectively, provide mask layout data which define the regions of wafer 28 to be illuminated. While such data can be provided in any format which defines the opaque and transparent regions of a mask, the data may conveniently be provided in the widely-used "GDS" format. Packages available for generating such data are available from various sources including Mentor Graphics of San Jose, California. These packages are commonly used at the "tape-out" stage of integrated circuit development.

In the conventional integrated circuit design process, the tape-out data in GDS format is provided to a reticle manufacturer. Thereafter, additional software is employed by the reticle developer to convert the tape-out data to a form that can control the position of an electron beam used in MEBS for generating the light and dark regions of the reticle. In the present invention, such additional software is unnecessary.

The data provided by the stations 32, 34, and 36 specifies the coordinates for a group of rectangles (or other shapes) which together make up the mask. This mask layout data is communicated to a server 40 containing the logic or protocol for queing, multiplexing, and otherwise providing the data to programmable reticle 24. Preferably, the server 40 also provides status information to the various stations. Server 40 ensures that conflicting information from two of stations 32, 34, and 36 is not sent to programmable reticle 24. For example, if a wafer is being exposed to a sequence of photolithography steps, server 40 ensures that each time a wafer is repositioned on support 30, the proper mask layout data for the "current level" of the integrated circuit is provided to programmable reticle 24.

The stations 32, 34, and 36, as well as server 40 may be personal computers, workstations, minicomputers, and mainframes. It should be understood that these machines may be manufactured by different vendors and may also run different operating systems such as MS-DOS, Microsoft Windows, Microsoft NT, various forms of UNIX, OS/2, MAC OS and others.

The stations 32, 34, and 36 are connected to server 40 via bi-directional lines and appropriate I/O circuitry. The bidirectional lines may be any suitable media such as coaxial cable, twisted pair wiring, fiber optic line, radio channels, and the like. Further, the network resulting from the interconnection of the lines may assume a variety of topologies, including ring, bus, star, and may include a collection of smaller networks linked by gateways and bridges.

It may often be the case that one or more of the stations is located remote from the programmable reticle. This is because the invention eliminates the need for a reticle formation step, thus allowing integrated circuit designers to provide layout data from their software directly to the programmable reticle. In most cases, the integrated circuit fabrication plant (employing the programmable reticle) is located some distance from the integrated circuit design facilities. In fact, the fabrication plant and the integrated circuit design facilities are often owned by a different enterprises.

In some cases, it will be necessary to include a fabrication administrator 42 to reprogram server 40 consistent with changes in the operational state of the integrated circuit fabrication plant. As shown, fabrication administration 42 communicates with server 40, thereby allowing the decisions of server 40 to be influenced or overridden by current requirements of the fabrication plant. In preferred embodiments, the fabrication administrator 42 will take the form of a user interface and associated logic for changing parameters of the server 40.

As should be apparent from the above discussion, the present invention affords considerable flexibility in adjusting the layout provided on a reticle. Thus, during the process of designing a new integrated circuit, corrections to errors can be made "on the fly" without resort to forming a new physical reticle. Referring back to Figure 1, this means that step 8 (preparation of a reticle of MEBS) can be illuminated. Thus, any necessary changes detected at decision step 14 of the process can be accounted for at design step 6, and more or less immediately transmitted to wafer fabrication plant. This is especially beneficial in the case where only a very small change must be made to an existing reticle. Previously when confronted with this situation, a designer or manufacturer would have to have a reticle manufacturer make an entirely new reticle by MEBS to correct the small error.

The present invention also provides another advantage at the manufacturing stage. First, as stated above, the reticle need not be physically replaced between each new mask step. Thus, the photolithography system processes wafers faster, thereby increasing throughput. Second, various regions of a given reticle may be provided with different mask layout patterns. Thus, some dies on a wafer will be exposed to one pattern while other dies on the same wafer will be exposed to a different pattern. Such arrangement is illustrated in Figure 3 where a reticle 50 is shown to include a first region 54 which provides the mask layout for dies of a first type on a given wafer. In addition, regions 56, 58, 60, and 62 each provide differing mask layouts for dies of multiple other types. This arrangement is particularly beneficial for custom chip manufactures which may

supply many different integrated circuits to their various customers. For example, if three different customers each require a different custom chip in small volumes, chips for all three orders may be fabricated on single chip by providing a reticle with three regions, each specifying a mask layout for one of the three customers. The different regions of the reticle are isolated with a stepper field as employed in conventional steppers.

It should also be noted that an arrangement such as that shown in Figure 3 also may be useful during the design and development of an integrated circuit. For example, it two or more designs require evaluation, mask layout patterns for each of those designs could be provided on the same reticle. Thus, on a single wafer, two or more designs could be fabricated and thereafter tested in parallel.

Although a few preferred embodiments of the present invention have been described in detail, it should be understood that the present invention may be embodied in many other specific forms without departing from the spirit or scope of the invention. Particularly, it should be understood that the programmable photolithography systems of this invention may be employed to pattern materials other than semiconductor substrates. For example, the principles of this invention can be applied to forming printed circuit boards, micromachined components such as micron-scale valves in stainless steel, etc. In addition, the invention can be employed in applications other than conventional "black and white" photolithography. For example, if a liquid crystal diode is employed in the programmable reticle, shades of gray and even colors may be employed to project additional information onto a radiation sensitive substrate. A gray element will transmit a fraction of the radiation transmitted by a transparent element, thereby only partially exposing a corresponding region of the substrate. In view of these alternatives, the present embodiments are to be considered as illustrative and not restrictive, and the invention is not to be limited to the details given herein, but may be modified within the scope of the appended claims.

CLAIMS

1. A lithography system for fabricating an integrated circuit on a semiconductor substrate, the lithography system comprising:

one or more stations for providing mask layout data defining features of said integrated circuit on said semiconductor substrate;

a programmable reticle in communication with said one or more stations and receiving said mask layout data, the programmable reticle having an array of elements each of which can be switched to either a transparent or opaque state in response to said mask layout data;

a radiation source for directing radiation through said elements of the programmable reticle that are in a transparent state, said radiation being blocked by the elements that are in an opaque state; and

an optical system for directing radiation passing through the programmable reticle onto a wafer containing a radiation-sensitive material and containing said semiconductor substrate, whereby regions of the wafer corresponding to the mask layout data are exposed to the radiation.

2. The lithography system of claim 1 having multiple stations, each configured to provide mask layout data.

3. The lithography system of claim 1 wherein at least one of the one or more stations includes a computer program for generating said mask layout data.

4. The lithography system of claim 1 wherein at least one of the one or more stations is provided at a location remote from the programmable reticle.

5. The lithography system of claim 1 further comprising a server in communication with said one or more stations and in communication with said programmable reticle, said server being adapted to receive said mask layout data, and then communicate that data to said programmable reticle according to a defined protocol.

6. The lithography system of claim 5 wherein said server is adapted to receive mask layout data from multiple stations simultaneously, and then queue that data according to said defined protocol.

7. The lithography system of claim 1 wherein said programmable reticle is a liquid crystal diode array.

8. The lithography system of claim 1 wherein the elements of the array have a largest dimension of at most about 10 micrometers.

9. The lithography system of claim 1 wherein the radiation source produces radiation in a frequency range selected from the group selected from the visible light, ultraviolet radiation, and x-ray radiation.

10. The lithography system of claim 1 wherein the optical system is a stepper.

11. The lithography system of claim 1 wherein the mask layout data is provided directly from a station in an enterprise which designed the integrated circuit.

12. A method for using lithography to fabricate integrated circuits on a semiconductor substrate, the method comprising the following steps:

programming a programmable reticle to define a mask layout, the programmable reticle having an array of elements each of which can be switched to either a transparent or opaque state in response to programming commands;

directing radiation onto said programmable reticle such that the radiation passes through said elements of the programmable reticle that are in a transparent state, and the radiation is blocked by the elements that are in an opaque state, thereby providing radiation in the pattern of the mask layout; and

directing the radiation pattern that passes through said programmable reticle onto a radiation sensitive layer on a wafer containing said semiconductor substrate to thereby expose the pattern of the mask layout on the radiation sensitive layer.

13. The method of claim 12 further comprising a step of removing either exposed regions or unexposed regions of said radiation sensitive layer to define a mask on said wafer.

14. The method of claim 13 further comprising a step of transforming unmasked regions of the wafer.

15. The method of claim 14 further comprising repeating the steps of (a) programming, (b) directing radiation onto said programmable reticle, (c) directing the radiation pattern onto the radiation sensitive layer, (d) removing regions of the radiation sensitive layer, and (e) transforming unmasked regions of the wafer to thereby form an integrated circuit.

16. The method of claim 15 wherein in the method of forming the integrated circuit, at least one time step (b) is replaced by a step of directing radiation onto a non-programmable reticle.

17. The method of claim 16 wherein the steps of directing radiation onto a non-programmable reticle are employed to form patterns for device elements on the semiconductor substrate, and the steps of directing radiation through the programmable reticle are employed to form interconnect patterns on the wafer.

18. The method of claim 12 further comprising a step of communicating mask layout data to said programmable reticle from a station having a program for generating said mask layout data, wherein said mask layout data includes instructions for programming said programmable reticle.

19. The method of claim 18 further comprising a step of queuing the mask layout data from multiple sources, including said station, in order to communicate that data to the programmable reticle in a defined order.

20. A lithography system for fabricating integrated circuits on a semiconductor substrate, the lithography system comprising:

data source means for providing mask layout data defining features of one or more integrated circuits on said semiconductor substrate;

programmable pattern generation means in communication with said data source means and receiving said mask layout data, the programmable pattern generation means having an array of elements each of which can be switched to either a transparent or opaque state in response to said mask layout data;

means for providing radiation such that said radiation is directed through said elements of the programmable pattern generation means that are in a transparent state, said radiation is blocked by the elements that are in an opaque state; and

means for directing radiation passing through the programmable pattern generation means onto a wafer containing a radiation-sensitive masking material and containing said semiconductor substrate, whereby the radiation exposes regions of the wafer corresponding to the mask layout data.

21. The lithography system of claim 20 wherein the programmable pattern generation means is a liquid crystal diode array.

22. The lithography system of claim 20 wherein the data source means includes one or more stations including a computer program means for generating said mask layout data.

23. The lithography system of claim 22 further comprising a server in communication with said one or more stations and in communication with said programmable pattern generation means, said server being adapted to receive said mask layout data, and then communicate that data to said programmable pattern generation means according to a defined protocol.

24. The lithography system of claim 20 wherein the elements of the programmable pattern generation means have a largest dimension of at most about 10 micrometers.

25. The lithography system of claim 20 wherein the means for providing radiation produces radiation in a frequency range selected from the group selected from the visible light, ultraviolet radiation, and x-ray radiation.

26. The lithography system of claim 20 wherein the means for directing radiation onto a wafer is a stepper.

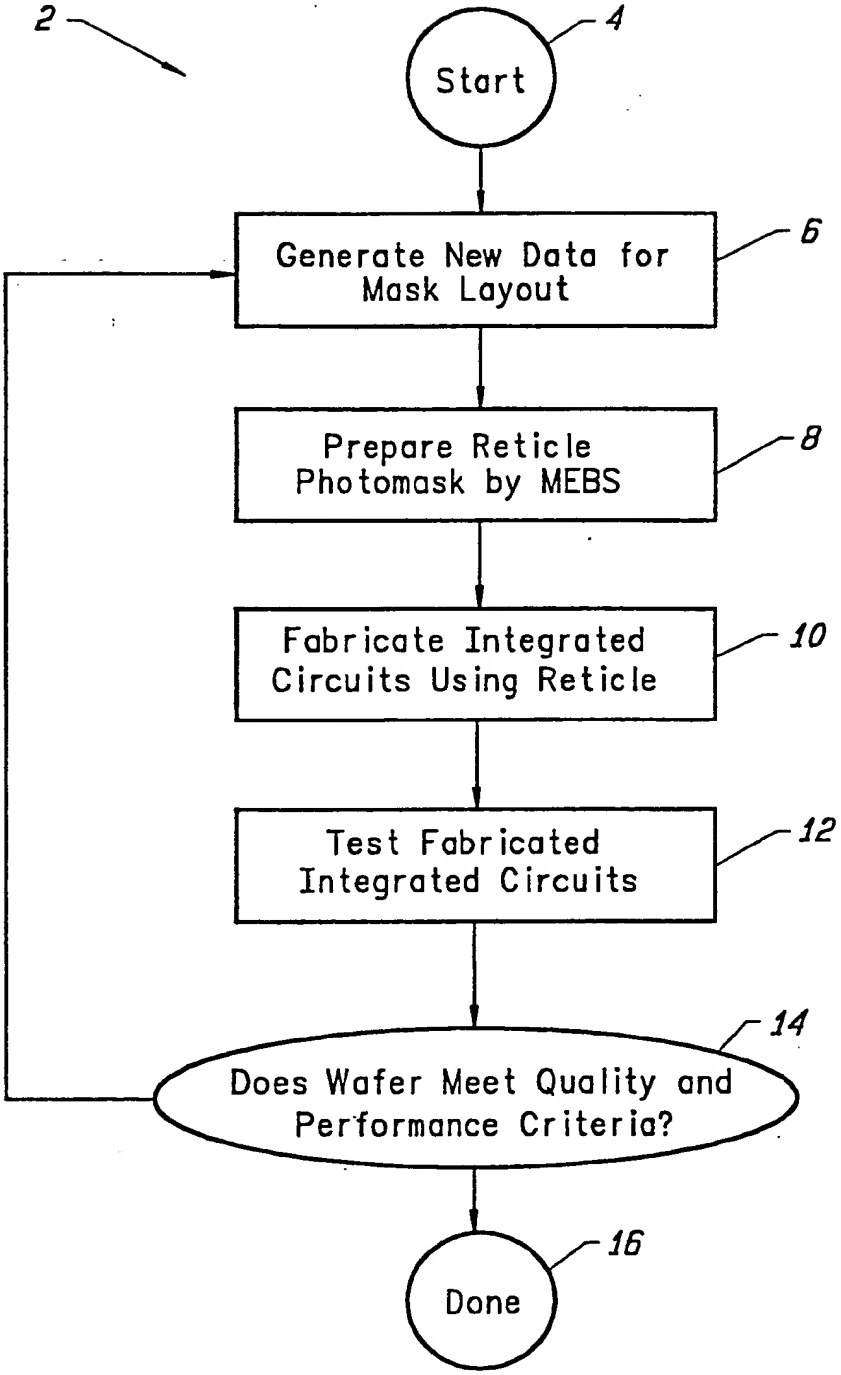
2
4
Start
Generate New Data for Mask Layout
6
Prepare Reticle Photomask by MEBS
8
Fabricate Integrated Circuits Using Reticle
10
Test Fabricated Integrated Circuits
12
Does Wafer Meet Quality and Performance Criteria?
14
Done
16

FIG. 1

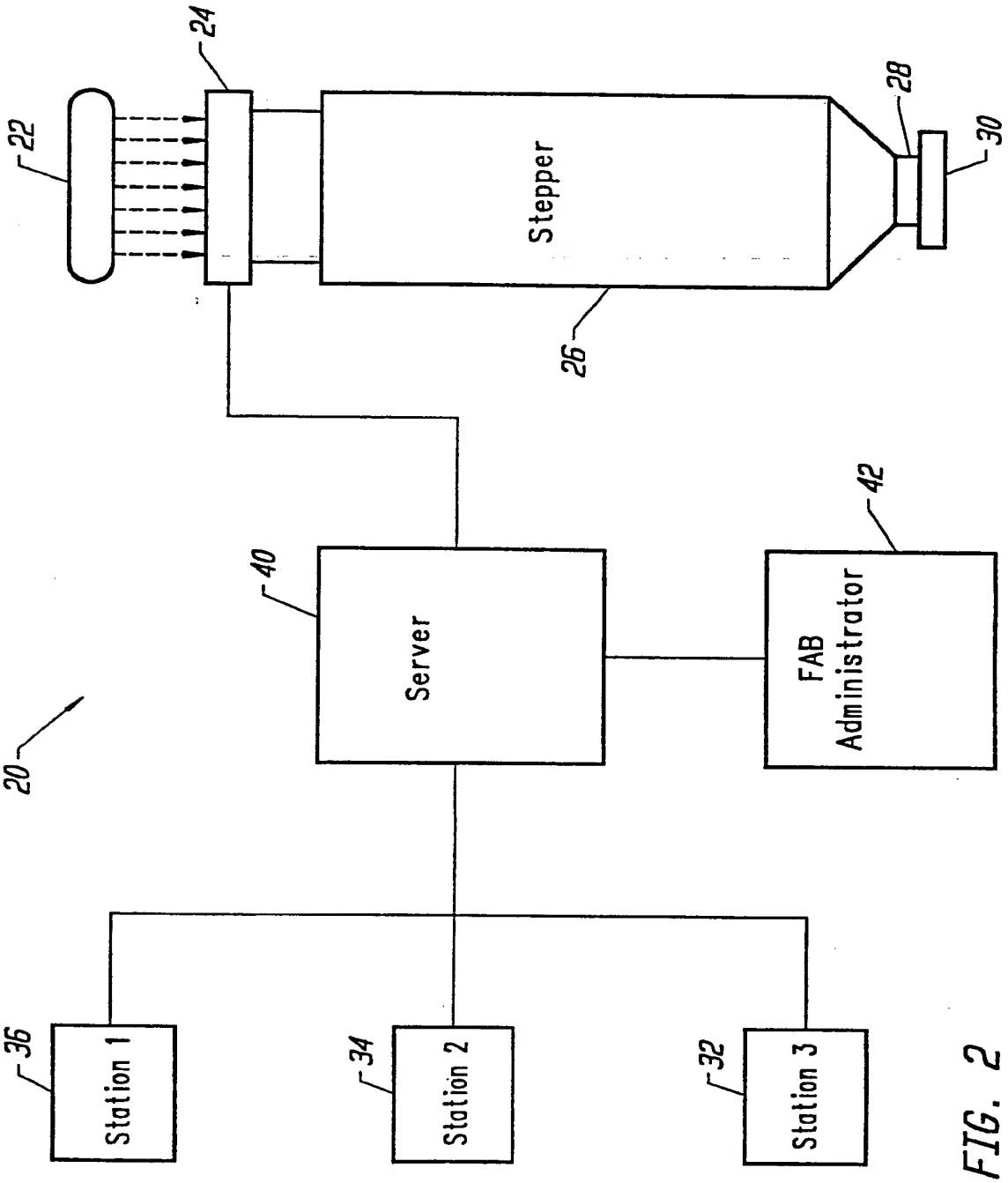
24
22
28
30
Stepper
26
40
Server
42
FAB
Administrator
20
36
Station 1
34
Station 2
32
Station 3

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US96/12330

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G03F 1/00, 7/00, 7/20
US CL :430/5, 20, 22, 312, 313; 355/40, 52, 71, 77; 359/40
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 430/5, 20, 22, 312, 313; 355/40, 52, 71, 77; 359/40

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

NONE

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

APS
search terms: mask, reticle, liquid crystal, semiconductor, integrated circuit, program

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US, A, 5,045,419 (OKUMURA) 3 September 1991, col. 2, lines 18-35.	1-26
X	US, A, 4,013,466 (KLAIBER) 22 March 1977, col. 9, line 59 to col. 10, line 49.	1-26
X	JP, A, 63-159853 (HITACHI LTD) 2 July 1988, Figs. 1-5.	1-26

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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30 AUGUST 1996	26 DEC 1996
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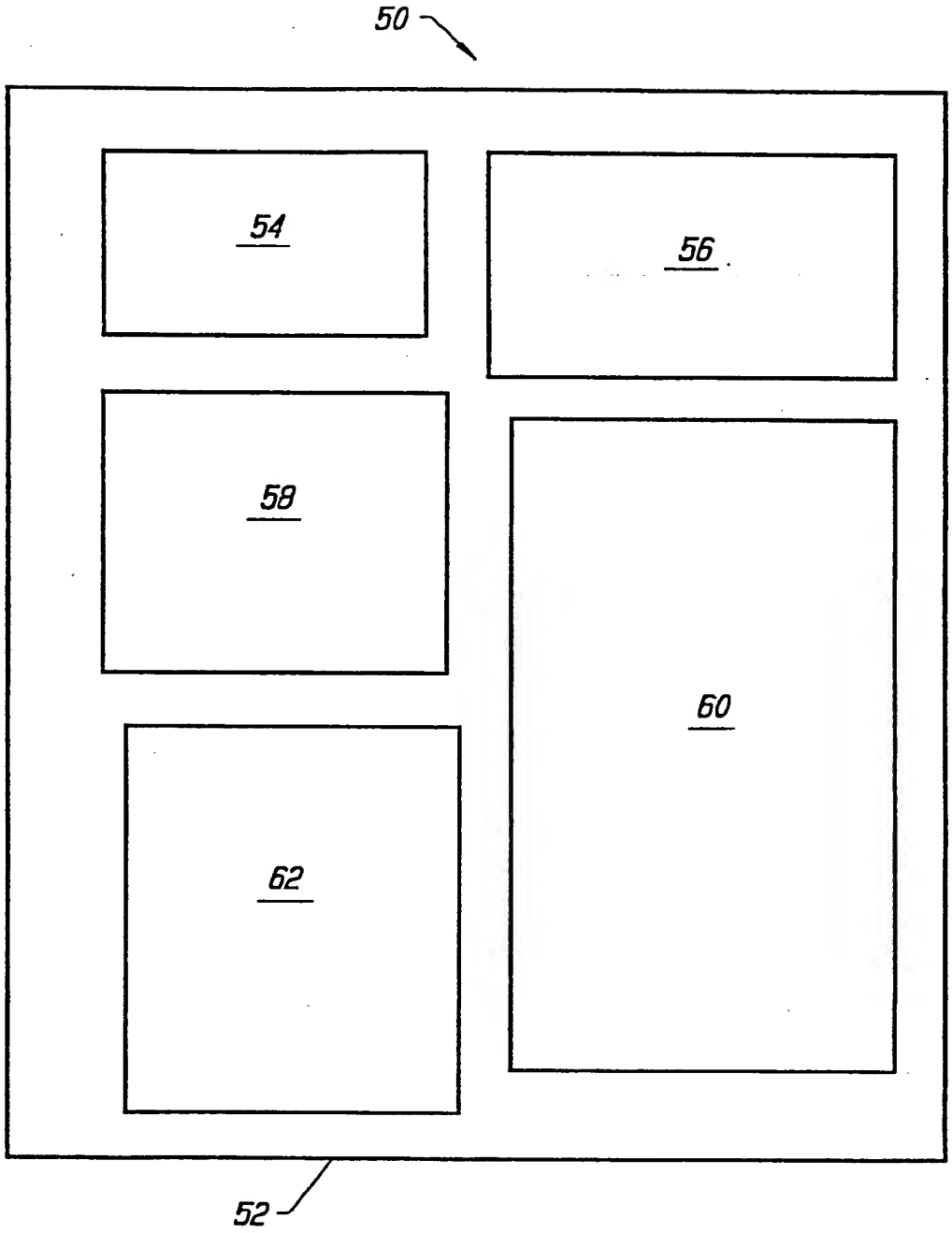

FIG. 3